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EXAMINER	
BUDD, PAUL A	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,201	CHANG, AUGUSTINE W.	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims **2-6,8,10-12,14,21-24,27-30,32-37,38-43** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims **2-6,8,10-12,14,21-24,27-30,32-37,38-43** all recite the limitation "software" or "software driven" or "dedicated programming facilities", but the specification does not contain any of said software or dedicated programming facilities and does not enable the use of "software" or "software driven" or "dedicated programming facilities".

Claim **15** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A Schottky Barrier Diode (SBD) cannot be a PN diode. The two devices are mutually exclusive. A Schottky Barrier Diode is the junction of a metal and a semiconductor. A PN diode is a junction of a p-type region with an n-type region. It is not possible for a

SBD to comprise a PN junction diode. The specification does not teach a way to resolve this contradiction nor does it teach any GaAs technologies.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim **1** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 7 of claim **1**, the limitation "with implementing macro functions" is vague and indefinite because it is not known what the structure "with implementing macro functions" is and how it is connected together. For the purposes of this Office Action the last limitation of claim **1** will be examined as "a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits". A method of operating a device cannot further limit a device or distinguish over the device.

Claims **4, 22,** and **35** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **4, 22,** and **35**, recite the limitation "wherein *software is provided to form reconfigurable logic gate array circuit units*". The claimed structure is indefinite and vague. Additionally the limitation "*reconfigurable*" adds additional uncertainly to what structure is being claimed since "*reconfigurable*" is inherently vague and changeable since no fixed structure has been defined.

Claims **5, 23,** and **36** recite the limitation "the single diagram" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims **1, 20,** and **33** make no reference to a "single diagram".

Claims **6, 24,** and **37** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **6, 24,** and **37**, recite the limitation "wherein the *software includes state tables, virtual machines, setup or initialization and test procedures, data access, transport, and storage algorithms.*" The claimed structure is indefinite and vague.

Claims **7, 25,** and **38** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **7, 25,** and **38**, recite the limitation "*wherein the circuit is hardware driven, wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and memory units, IO transceivers, and terminators*". The claimed structure is indefinite and vague.

Claims **8, 26,** and **39** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **8, 26,** and **39**, recite the limitation "*wherein the hardware comprises software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch transistor is of VT type.*" The claimed structure is indefinite and vague.

Claims **9, 27,** and **40** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **9, 27,** and **40**, recite the limitation "*which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit act as analog signal comparator.*" The claimed structure is indefinite and vague.

Claims **9, 27,** and **40** recite the limitation "the switch transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims **1,7,20,25,33,** and **38** make no reference to a "switch transistor".

Claims **10, 28,** and **41** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **10, 28,** and **41**, recite the limitation "*which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL gate may perform a nonvolatile latch function.*" The claimed structure is indefinite and vague.

Claims **10, 28,** and **41** recite the limitation "the switch transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims **1, 7, 20, 25, 33,** and **38** make no reference to a "switch transistor".

Claims **11, 29,** and **42** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **11, 29,** and **42**, recite the limitation "*which includes software driven SCL gate arrays, IO transceivers, terminators,*

capacitors, wherein the switch transistor is of VT type, and the SCL unit may process multi-value logic operation with binary, ternary and quaternary operators." The claimed structure is indefinite and vague.

Claims **11, 29,** and **42** recite the limitation "the switch transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims **1, 7, 20, 25, 33,** and **38** make no reference to a "switch transistor".

Claims **12, 30,** and **43** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **12, 30,** and **43**, recite the limitation "*which includes software driven CMOS-TTL gate arrays, IO transceivers, terminators and capacitors.*" The claimed structure is indefinite and vague.

Claims **14** and **32** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims **14** and **32**, recite the limitation "*dedicated programming facilities*". This limitation is vague and indefinite because it is unknown what additional structural limitations are embodied by the limitation "*dedicated programming facilities*".

Claim **15** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim **15**, recites the limitation "wherein the SBDs comprise a PN junction diode if SOI GaAs technologies are used." It is not known whether or not "SOI GaAs technologies" is a limitation and if so what comprises the claimed diode

structure since as above a Schottky diode and a PN diode are structurally exclusive devices. Claim **15** cannot be searched because of the contradictory nature of the claimed structure.

Claim **17** recites the limitation "the well" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. Claim **1** makes no reference to a "well". Claim **17** cannot be searched.

Claim **18** recites the limitation "the well" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Claim **1** makes no reference to a "well". Claim **18** cannot be searched.

Claim **19** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim **19**, recites the limitation "wherein the SBDs are adaptable to other product applications including but not limited to DRAM, Flash, CAM, PLD, ROM, and embedded ASICs." It is not know what the structure being claimed is and how the Schottky Barrier Diodes are connected to any additional structures.

Claim **20** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 7-9 of claim **20**, the limitation "*with implementing macro functions, wherein the circuit is software driven and wherein the at least a portion of the macro functions can be hardwired macroassets*" is vague and indefinite because it is not known what structure the limitation "*with implementing macro functions, wherein the circuit is software driven and wherein the at least a portion of the macro functions can*

be hardwired macroassets." is and how it is connected together. The Office recommends the structure embodied by the limitations be described in structural terms to render them definite. For the purposes of this Office Action the last limitation of claim **20** will be examined as "a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits". A method of operating a device cannot further limit a device or distinguish over the device.

Claim **33** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 7-9 of claim **33**, the limitation "*with implementing macro functions, wherein a part of the elements are user programmed and part of the elements are factory programmable, wherein the circuit is software driven*" is vague and indefinite because it is not known what structure the limitation "*with implementing macro functions, wherein a part of the elements are user programmed and part of the elements are factory programmable, wherein the circuit is software driven.*" is and how it is connected together. The Office recommends the structure embodied by the limitations be described in structural terms to render them definite. For the purposes of this Office Action the last limitation of claim **33** will be examined as "a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits". A method of operating a device cannot further limit a device or distinguish over the device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-14,** and **19-43** rejected under 35 U.S.C. 102(e) as anticipated by Bhattacharyya et al. (US Pat. Pub. 2005/0099839) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bhattacharyya et al. (US Pat. Pub. 2005/0099839).

Regarding claims **1,20,** and **33** Bhattacharyya teaches a mixed signal circuit comprising:

a plurality of fixed threshold [FIG.s 7-8; 50, page 6 sections 0090-0096] and variable threshold [FIG. 22C-23; page 15-16, section 0229-0241] transistors;

a plurality of Schottky barrier diodes [FIG. 22C, 864, 868; page 15, sections 0227, 0229, 230];

a plurality of poly silicon film resistors [FIG. 41, 1812, page 25 section 0343; also: FIG 17, 612; page 12 section 0193, The conductive pedestal is n+doped and optionally made of polysilicon. This conductive pedestal made of doped polysilicon is inherently a polysilicon resistor];

a plurality of capacitors [FIG. 8; 90, page 7 sections 0100-0102; page 25, section 0343]; and

a plurality of wiring tracks [FIG. 19, 720, 687, 722; page 13, section 0203], wherein all of the elements are on a single substrate [FIG. 41] to form integrated circuits *with implementing macro functions*. On page 23 section 0324 Bhattacharyya teaches that "Various of the devices described with reference to FIGS. 1-38 can be incorporated into a SID... and/or can be interconnected in planar configuration (FIG. 41)". Thus Bhattacharyya teaches forming on a single substrate any combination of the devices taught in FIGS. 1-38. From page 23 section 0322, until page 25 section 0347, Bhattacharyya teaches integration of devices in figures 1-38 into a single substrate.

As for claim **20's** *additional limitation beyond claim* **1**:

"a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits *with implementing macro functions, wherein the circuit is software driven and wherein the at least a portion of the macro functions can be hardwired macroassets."* The intended use limitation "*wherein the circuit* ***is software*** *driven and wherein the at least a portion of the macro functions can be hardwired macroassets*." does not distinguish over the rejection of claim **1** above. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1**.

As for claim **33's** *additional limitation beyond claim* **1**:

"a plurality of wiring tracks, wherein all the elements are on a single substrate to form integrated circuits *with implementing macro functions, wherein a part of the elements are user programmed and part of the elements are factory programmable, wherein the circuit is* ***software*** *driven".* The intended use limitation "*with implementing macro functions, wherein a part of the elements are user programmed and part of the elements are factory programmable, wherein the circuit is* ***software*** *driven*." does not distinguish over the rejection of claim **1** above. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1**.

Regarding claim **2**, Bhattacharyya teaches the mixed signal circuit of claim **1** wherein *the circuit is* ***software*** *driven*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1**.

Regarding claims **3, 21,** and **34** Bhattacharyya teaches the mixed signal circuit of claim **2** wherein ***software*** *is provided to adjust the threshold of the variable threshold transistors*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** rejection above these additional

intended use limitations do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claims **4, 22,** and **35** Bhattacharyya teaches the mixed signal circuit of claim **2** wherein ***software*** *is provided to form reconfigurable logic gate array circuit units*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claims **5, 23,** and **36** Bhattacharyya teaches the mixed signal circuit of claim **2** wherein *software is provided to complete certain network connections among various units in the single diagram*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). These additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claims **6, 24,** and **37** Bhattacharyya teaches the mixed signal circuit of claim **2** wherein the *software includes state tables, virtual machines, setup or initialization and test procedures, data access, transport, and storage algorithms. Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). These additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claim **7, 25,** and **38**, Bhattacharyya teaches the mixed signal circuit of claim **1** (or **20** or **33**) wherein the circuit is *hardware driven*, wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and memory units, IO transceivers, and terminators. *Intended use (hardware driven) does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). Bhattacharyya teaches [pages 23-25 sections 0325-0347] how his device may include a signal generator, a smart identity/data device, a receiver, transmitter, system on chip, modulators, detectors, wave-guides, actuators, sensors, switches, optical sensors, micro-electro-mechanical systems, RFIDs, photodiodes, CMOS transistors, DRAM cells, ROM cells, FLASH cells, CMOS inverters, thyristors, bipolar transistors, non-volatile storage devices, a processor, resistors, capacitors, inductors, controllers, Schottky diodes, digit print sensing devices, as well as other devices. As such, it is considered obvious that the invention be applied to hardwired Schottky CMOS Logic (SCL) gate array and memory units, or IO transceivers, or terminators as these are all well known applications of the above devices or merely obvious variants in which the teachings of Bhattacharyya et al. may be applied.

Regarding claim **8, 26,** and **39**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25** or **38**) wherein the hardware comprises ***software*** *driven* SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch transistor is of VT type. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641

(CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claim **9, 27,** and **40**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25** or **38**) which includes ***software** driven* SCL gate arrays, IO transceivers, terminators, capacitors, wherein ***the switch transistor*** is of VT type, and the SCL unit *act as analog signal comparator*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claim **10, 28,** and **41**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25** or **38**) which includes ***software** driven* SCL gate arrays, IO transceivers, terminators, capacitors, wherein ***the switch transistor*** is of VT type, *and the SCL gate may perform a nonvolatile latch function*. *Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional intended use limitations do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claim **11, 29,** and **42**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25** or **38**) which includes ***software** driven* SCL gate arrays, IO

transceivers, terminators, capacitors, wherein ***the switch transistor*** is of VT type, and the SCL unit *may process multi-value logic operation with binary, ternary and quaternary operators. Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional intended use limitations do not distinguish over the structure taught in claim **1** (or **20** or **33**).

Regarding claim **12, 30,** and **43**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25** or **38**) which *includes **software** driven CMOS-TTL gate arrays, IO transceivers, terminators and capacitors. Intended use does not avoid prior art*: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20** or **33**). Bhattacharyya teaches [pages 23-25 sections 325-0347] how his device may include a signal generator, a smart identity/data device, a receiver, transmitter, system on chip, modulators, detectors, wave-guides, actuators, sensors, switches, optical sensors, micro-electro-mechanical systems, RFIDs, photodiodes, CMOS transistors, DRAM cells, ROM cells, FLASH cells, CMOS inverters, thyristors, bipolar transistors, non-volatile storage devices, a processor, resistors, capacitors, inductors, controllers, Schottky diodes, digit print sensing devices, as well as other devices. As such, it is considered either anticipated or obvious that the invention be applied to "*CMOS-TTL gate arrays, IO transceivers, terminators and*

capacitors" as these are all well known applications of the above devices or merely obvious variants in which the teachings of Bhattacharyya et al. may be applied.

Regarding claim **13,** and **31**, Bhattacharyya teaches the mixed signal circuit of claim **7** (or **25**) which includes hardwired conventional logic and memory units including but not limited to CMOS-TTL gate arrays, Register files, embedded RAM, ROM and Flash cores. Bhattacharyya teaches [pages 23-25 sections 325-0347] how his device may include a signal generator, a smart identity/data device, a receiver, transmitter, system on chip, modulators, detectors, wave-guides, actuators, sensors, switches, optical sensors, micro-electro-mechanical systems, RFIDs, photodiodes, CMOS transistors, DRAM cells, ROM cells, FLASH cells, CMOS inverters, thyristors, bipolar transistors, non-volatile storage devices, a processor, resistors, capacitors, inductors, controllers, Schottky diodes, digit print sensing devices, as well as other devices. As such, it is considered either anticipated or obvious that the invention be applied to *"conventional logic and memory units including but not limited to CMOS-TTL gate arrays, Register files, embedded RAM, ROM and Flash cores*" as these are all well known applications of the above devices or merely obvious variants in which the teachings of Bhattacharyya et al. may be applied.

Regarding claim **14,** and **32**, Bhattacharyya teaches the mixed signal circuit of claim **7** which *includes* ***dedicated programming facilities*** *of voltage and current sources, clock and oscillators, state machines and counters, to implement and control*

both cell wise and block wise cell operations and which is shared to alter the charge storage or VT threshold of the selected device(s) in the logic and (Flash) memory circuitry. Intended use does not avoid prior art: In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974). In addition to the **112(1st)** and 112(2nd) rejections above these additional *intended use limitations* do not distinguish over the structure taught in claim **1** (or **20**).

Regarding claim **19**, Bhattacharyya teaches the mixed signal circuit of claim **3** wherein the SBDs are adaptable to other product applications including but not limited to DRAM, Flash, CAM, PLD, ROM, and embedded ASICs. There is nothing about the SBDs taught by Bhattacharyya that would prevent his SBDs from being adaptable to DRAM, Flash, CAM, PLD, ROM, and embedded ASICs.

Bhattacharyya teaches [pages 23-25 sections 0325-0347] how his device may include a signal generator, a smart identity/data device, a receiver, transmitter, system on chip, modulators, detectors, wave-guides, actuators, sensors, switches, optical sensors, micro-electro-mechanical systems, RFIDs, photodiodes, CMOS transistors, DRAM cells, ROM cells, FLASH cells, CMOS inverters, thyristors, bipolar transistors, non-volatile storage devices, a processor, resistors, capacitors, inductors, controllers, Schottky diodes, digit print sensing devices, as well as other devices. As such, it is considered either anticipated or obvious that the invention be applied to "wherein the SBDs are adaptable to other product applications including but not limited to DRAM, Flash, CAM, PLD, ROM, and embedded ASICs. There is nothing about the SBDs

taught by Bhattacharyya that would prevent his SBDs from being adaptable to "*DRAM, Flash, CAM, PLD, ROM, and embedded ASICs.*" as these are all well known applications of the above devices or merely obvious variants in which the teachings of Bhattacharyya et al. may be applied.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim **16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya et al. (US Pat. Pub. 2005/0099839) in view of Voldman et al. (US Patent 6,433,985).

Regarding claim **16**, Bhattacharyya teaches the mixed signal circuit of claim **1** but does not explicitly disclose, "wherein the SBD can be coupled to input pads for Electrical Static Discharge protection." Voldman teaches, [FIG. 1, 102, column 2, lines 20-40], an ESD protection circuit which comprises a SBD coupled to input pads for ESD protection. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a SBD as an ESD protection device for the purpose that it "prevents high voltage oxide stress" [column 1, lines 30-31]. These references

are analogous art because they both address the issue of protecting internal circuits from ESD stress events.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAB

JEROME JACKSON
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